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Drafts
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11: (226283) micron or microns or um
12: (55240) micrometer or micrometers
13: (303753) electrode or electrodes
14: (988573) via or vias
15: (27316) trench or trenches
16: (264198) 11 or 12
17: (1179557) 13 or 14 or 15
18: (31031) 16 same 17
19: (34375) DRAM
110: (1563) 18 and 19
111: (7246) 16 nears 17
112: (561) 19 and 111
114: (2693298) @ack19980722
115: (360) 112 and 114

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U	PT	P	Document ID	Issue Date	Pages	Title	Current OR	Current Ref	Retrieval C	Inventor	S	C	3
1			US 6570550 B1	20030527	25	Active matrix liquid crystal image generator	345/89	345/97		Hande, Mark A. et al.			
2			US 6559825 B2	20030506	46	Display system for wireless pager	345/102	340/7.32		Jacobsen, Jeffrey et al.			
3			US 6518155 B1	20030211	18	Device structure and method for reducing silicide	438/592	438/595		Chau, Robert S. et al.			
4			US 6486862 B1	20021126	55	Card reader display system	345/88	345/87		Jacobsen, Jeffrey et al.			
5			US 6465865 B1	20021015	8	Isolated structure and method of fabricating such a	257/506	257/306		Gonzalez, Fernando			
6			US 6407044 B2	20020618	11	Aerosol personal cleansing emulsion compositions which	510/140	424/401		Dixon, Thomas Jefferson			
7			US 6376369 B1	20020423	13	Robust pressure aluminum fill process	438/643	438/618		Doan, Trung T.			
8			US 6320261 B1	20011120	15	High aspect ratio metallization structures for	257/754	250/382		Burton, Randle D. et al.			
9			US 6319542 B1	20011120	10	Lightly donor doped electrodes for	427/79	257/821.272		Summerville, Scott R. et al.			
10			US 6317112 B1	20011113	23	Active matrix liquid crystal image generator with hybrid	345/89	345/102		Hande, Mark A. et al.			
11			US 6303493 B1	20011016	20	Wiring for semiconductor device and method for	438/652	257/823.019		Lee, Chang Jae			
12			US 6297129 B1	20011002	9	Methods of forming integrated circuitry, and	438/439	257/305		Tran, Luan et al.			

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Detailed Description Text - DPMX (9):

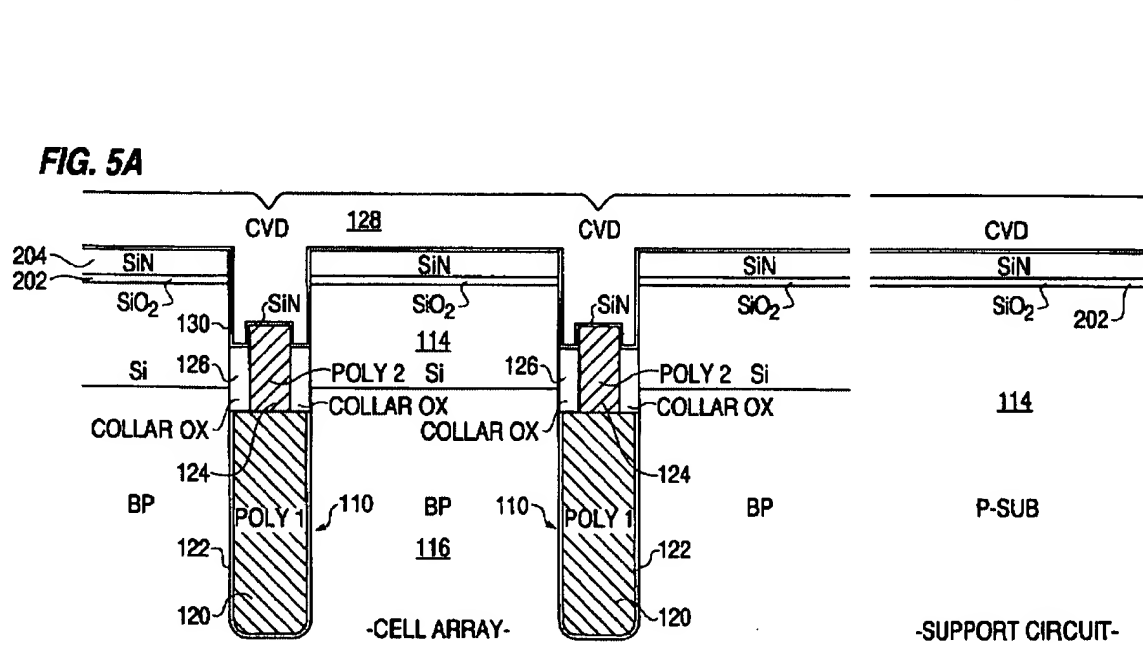
With reference to FIG. 5D, a pad oxide layer 210 of silicon dioxide (SiO₂, sub.2) and a pad nitride layer 212 of silicon nitride (Si₃N₄, sub.4) are successively formed on the surface of epitaxial silicon layer 208. Pad oxide layer 210 may be formed by thermal oxidation (e.g., 900.degree. C. in an atmosphere of dry O₂, sub.2) and may have a thickness of about 10 nanometers. Pad nitride layer 212 may be formed by chemical vapor deposition and may have a thickness of about 100 nanometers. Shallow trenches 214 are then formed in epitaxial layer 208 using a patterned resist (not shown) and an etching process such as reactive ion etching (RIE). The dimensions of the shallow trenches are dependent upon feature size. For example, for a 1 Gbit DRAM, shallow trenches 214 may have a width of 0.15 micrometers (μm), a depth of 0.15 micrometers (μm), an insulating layer of, for example, TEOS, is then blanket deposited over the surface of pad nitride layer 212 and in shallow trenches 214. The insulating layer is then etched back using, for example, CMP and RIE, with pad nitride layer 212 serving as a stopper layer, whereby shallow trench isolation structures 108 which define the active areas AA are formed.

Detailed Description Text - DPMX (17):

In the second embodiment, deep trenches 110 are oriented in a direction which is orthogonal to the direction in which the deep trenches 110 are oriented in the first embodiment. Because of this, forming the semiconductor memory device of FIGS. 6 and 7 using the method described with respect to FIGS. 5A-5I will cause the transfer transistors to be formed in the portion of the epitaxial layer over the deep trench. As noted above, this portion of the epitaxial layer may have defects which could adversely affect the operation of the transfer transistors. In order to provide a high quality epitaxial layer in which to form the transfer transistors, the epitaxial layer may be subjected to a high temperature annealing process (e.g., at a temperature of about 1100.degree. C. in an atmosphere of N₂, sub.2). Alternatively, a laser or an electron beam anneal may be used. In still another alternative embodiment, a water bonding technique such as that shown in FIG. 8 may be utilized. Specifically, a first silicon wafer 302 having the trench capacitors formed therein is bonded to a second silicon wafer 306 having shallow trench isolation regions 108 formed therein. Second silicon wafer 306 is then polished by, for example, chemical mechanical polishing (CMP) to provide a silicon layer 308 having a thickness of, for example, about 0.15 micrometers (μm), for a 1 Gbit DRAM. The process steps of FIGS. 5E-5I may then be carried out to form the semiconductor memory device of FIGS. 6 and 7. In this way, the problems associated with low quality epitaxial films grown over the deep trenches can be avoided.

Detailed Description Text - DPMX (19):

Table 1 provides a cell comparison for the first generation of 1 Gbit DRAM devices having a 0.18 micron design rule. As can be seen from the data set forth in Table 1, DRAM devices manufactured in accordance with the embodiments of the present invention provide the same capacitance as scaled down cells manufactured in accordance with the M1NT architecture shown in FIGS. 1A and 1B of this patent application, while at the same time providing trenches with smaller aspect ratios within which the capacitors are formed. Specifically, 1 Gbit memory cells in accordance with the first and second embodiments of the present invention have trench capacitors formed in trenches with aspect ratios which are 28% less than the aspect ratio of the trenches for 1 Gbit memory cells based on scaling down the current M1NT architecture. Memory cells in accordance with the third embodiment of the present invention have trench



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US-PAT-NO: 6259127

DOCUMENT-IDENTIFIER: US 6259127 B1

TITLE: Integrated circuit container having partially rugged

01/1/72) SURFACE DRAINS

Application Filing Date - AD (1) :
19980430

19980430

Brief Summary Text - BSTX (5):

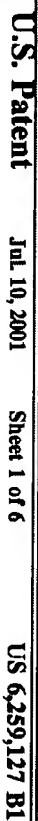
FIG. 1, for example, illustrates a container capacitor structure 10 for a DRAM memory cell. An insulating or dielectric layer 12, such as boron phosphosilicate glass (BPSG), is planarized and patterned with a photo lithographic mask. The dielectric layer 12 is then etched through the resist mask 24 between a pair of gate electrodes 14 to an underlying silicon substrate, thus forming the container structure 10. The etch may select against nitride insulation of the gate electrodes 14, for example, including nitride sidewall spacers 22. The container 10 is essentially a cylindrical cavity, but it is illustrated in FIG. 1 in schematic cross-section, for simplicity, without showing the backwall of the cylinder. A conductive layer (not shown in FIG. 1) would then be conformally deposited over the walls of the container 10 to serve as the bottom plate. The interlayer dielectric and top plate would be successively deposited over the bottom plate, forming a capacitor.

Brief Summary Text - BSTX (7) :

At the same time, the formation of HSG also increases the thickness of the bottom plate, generally by more than 500 .ANG. and often closer to 600 .ANG.. For the container structure 10 of FIG. 1, this added thickness over the container walls still leaves adequate space within the container 10 for additional layers in an upper portion 19. The added thickness may become critical, however, at a bottom portion 20 of the container 10, which is narrowly confined between the gate electrodes 14. In high-density DRAM chips, the pair of gate electrodes 14 are less than 0.35 microns (3,500 .ANG.) apart. Sidewall spacers 22, which isolate the gate electrodes 14 from the capacitor to be formed, occupy 700 .ANG. on either side of the container 10 cross-section, leaving a diameter of only about 2,100 .ANG. for the remainder of the capacitor structure within the bottom portion of the container 10. Phase 2,100 .ANG. may easily be filled by the bottom plate to be formed of an amorphous or polysilicon layer (about 500 .ANG. around the container circumference) and the HSG formed over the silicon layer (about 600 .ANG.). These thicknesses represent reductions in the radius of the container and must be doubled in calculating the reduction of the container diameter.

Detailed Description Text - DETX (2) :

Although the present description focuses on the context of a DRAM cell, it will be understood that the present invention may have utility in many applications where a conductive layer of rough or high surface area is desired. Such applications include capacitors of all sorts, and especially capacitors



Document ID	Page	U	S	C	P	Kind Codes	Source
US 6187152 B1	21						USPAT
US 6183611 B1	21						USPAT
US 6165956 A	8						USPAT
US 609702 A	5						USPAT
US 5865679 A	125						USPAT
US 5907791 A	11						USPAT
US 5865657 A	22						USPAT

Brief Summary Text - B97X (7):

One problem with this system is that often substantial time (e.g., minutes) elapses between the electroplating in the plating cell and the rinsing while the system awaits availability of a rinse cell, a transport system, or a human operator. Substantial time may elapse when, for example, there is throughput bottleneck in the rinse stage. During this time, solution molecules may stay attached to the wafer due to the relatively low surface energy of the solution. This allows the solution, in some cases, to chemically react with the elements of the wafer, particularly metallic elements. For example, a water-based salt solution tarnishes a copper work piece if exposed even for a short time. As circuit feature dimensions progress farther into the submicron range, such tarnishing can significantly reduce die yields.

Brief Summary Text - B97X (12):

The following occurs within this single plating cell. A wafer is first electroplated by lowering the wafer holder to a position in the inner plating bath container that is below a plating solution level. After electroplating, the wafer is raised out of the plating bath and spun so that the spin-off water and plating solution enters the reclaim or waste inlets. When the spin-off water and plating solution enters the waste inlet, a relatively large volume of rinse solution (e.g., 10 milliliters or more) can be applied (e.g., sprayed) onto the wafer to thoroughly rinse the wafer. The wafer can also be subsequently dried by spinning the wafer at a relatively fast spin rate.

Detailed Description Text - D97X (2):

The principles of the present invention solve the problem of time lag between the plating and rinse stages by providing a plating cell that performs both plating and full rinse. Performing both plating and full rinse would be undesirable in the prior art plating cell at least because the full rinse would cause rapid dilution of the electroplating solution. The plating cell may also have the ability to perform pre-wetting.

Detailed Description Text - D97X (8):

Electroplating may be performed in circulation mode as follows. In response to an instruction on instruction terminal 199, actuator 170 positions wafer holder 190 so that wafer W is held in solution S, for example, at position 1. A current source 192, disposed within the inner plating bath container 110, emits current through solution S and into wafer W. This causes metal to form on the surface of wafer W as the metal salts within the solution S reduce.

Detailed Description Text - D97X (13):

Once the wafer W has been thoroughly rinsed, the wafer W can be spun to dry at a spin rate of, for example, from 400 to 800 RPM. Therefore, within a very short period after the completion of electroplating, the wafer W is thoroughly rinsed and dried. Therefore, the wafer W is not exposed to corrosive elements as long as the wafer W might be in the prior art.

Detailed Description Text - D97X (15):

Cell 100 may also be used for pre-wetting by spraying a wetting solution (e.g., ultra pure water) onto the wafer W before electroplating while the wafer is positioned over inner plating bath container 110.

United States Patent [19]

Reid et al.

(11) Patent Number: 6,099,702
(45) Date of Patent: Aug. 8, 2000

[54] ELECTROPLATING CHAMBER WITH ROTATABLE WAFFER HOLDER AND PRE-WETTING AND RINSING CAPABILITY

[75] Inventors: Jonathan D. Reid, Sherwood, Steven W. Thayer, West Linn, Robert J. Combs III, Lake Oswego, Evan E. Fulton, Portland, all of Oreg.

[73] Assignee: Novellus Systems, Inc., San Jose, Calif.

[12] Appl. No.: 09/096,015

[22] Filed: Jun. 10, 1998

[51] Int. Cl.⁷ C25D 17/06; C25D 21/08

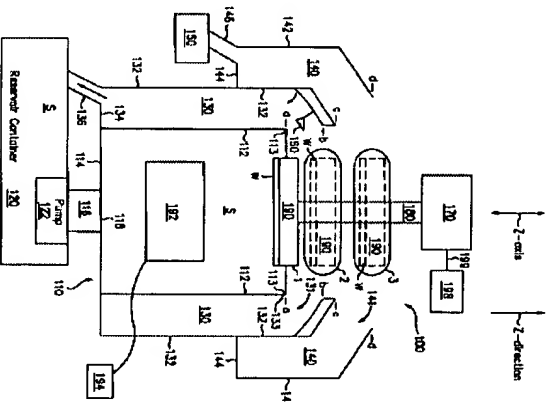
[52] U.S. Cl. 204/212; 118/52; 118/400; 118/500; 204/224 R; 204/225; 204/237; 204/275

[58] Field of Search 205/122, 204/212, 204/224 R, 225, 237, 275; 118/400, 416, 52, 400, 500, 501

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10 Claims, 1 Drawing Sheet



DOCUMENT-IDENTIFIER: US 6165956 A

TITLE: Methods and apparatus for cleaning semiconductor substrates after polishing of copper film

KWIC -----

Application Filing Date - AD (1):
19971021

Brief Summary Text - BBTX (6):
One process for Cu metalliz

One process for Cu metallization uses a dual damascene approach. As illustrated in FIG. 1a, a dielectric layer 110 is deposited above a substrate 100. Dielectric layer 110 may be made up of materials such as silicon dioxide. Vias and/or trenches 120 are then formed in the dielectric layer 110, as illustrated in FIG. 1b. Vias/trenches 120 may be formed, for example, using dry etching techniques. Next, a thin layer of barrier material (barrier layer) 130, for example, tantalum (Ta), titanium (Ti), or titanium nitride (TiN) is deposited as illustrated in FIG. 1c. After barrier layer 130 is deposited in the vias/trenches 120 are filled with copper (Cu) layer 140, as illustrated in FIG. 1d. Copper layer 140 may be deposited using well known deposition techniques such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or electroplating. In order to isolate the copper interconnects, as illustrated in FIG. 1e, the excess copper layer 140 and barrier layer 130 must be removed.

Detailed Description Text - DENV (11):
After the second scrub the substrate is then automatically removed from the inside brush station 230 and placed into the rinse, spin and dry station 240. Rinse, spin, and dry station 240 rinses, spins, and dries the substrate. At this point the water has been cleaned.

United States Patent [19]
Zhang et al.

(11) Patent Number: 6,165,956
(45) Date of Patent: Dec. 26, 2000

[54] METHODS AND APPARATUS FOR CLEANING SEMICONDUCTOR SUBSTRATES AFTER POLISHING OF COPPER FILM

[75] **Inventors:** Liming Zhang, Tucson, Ariz.; Yuetting Zhao, Santa Clara, Calif.; Diane J. Hynes, San Jose, Calif.; Wilbur C. Kuttell, Palo Alto, Calif.

[73] Assignee: Lam Research Corporation, Fremont, Calif.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: 08/934,393

[51] **Int. Cl.⁷** CLASSIFICATION CODE **C11D 9/04; C11D 17/08;**
C11D 15/00

U.S. Cl. 510/175; 510/176; 510/435;
[52]

[58] **Field of Search** 510/434, 254,
510/175, 176, 257, 488, 435; 134/3, 41.

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(11) Patent Number: 6,165,956
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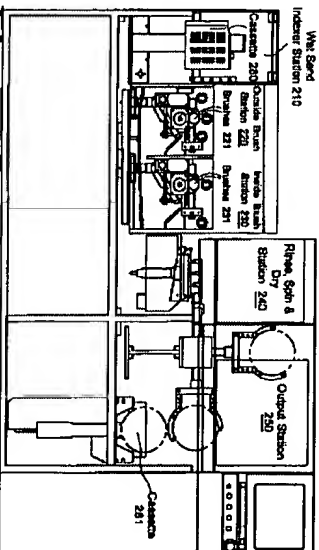
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Assistant Examiner—Gregory E. Webb
Attorney, Agent, or Firm—Martine Penilla & Kim, LLP

ABSTRACT

A cleaning solution, method, and apparatus for cleaning semiconductor substrates after their chemical-mechanical polishing of copper films is described. The present invention includes a cleaning solution which combines deionized water, an organic compound, and a fluoride compound in an acidic pH environment for polishing the surface of a semiconductor substrate after depositing a copper layer. Such methods of cleaning semiconductor substrates after copper CMP alleviate the problems associated with brush loading and surface and subsurface contamination.

1 Claim, 4 Drawing Sheets



prior to the effective date of the reference(s) or the activity. Such evidence is sufficient because applicant's possession of what is shown carries with it possession of variations and adaptations which would have been obvious, at the same time, to one of ordinary skill in the art. However, the affidavit or declaration showing must still establish possession of the invention (i.e., the basic inventive concept) and not just of what one reference (in a combination of applied references) happens to show, if that reference does not itself teach the basic inventive concept. *In re Spiller*, 500 F.2d 1170, 182 USPQ 614 (CCPA 1974) (Claimed invention was use of electrostatic forces to adhere dry starch particles to a wet paper web on the Fourdrinier wire of a paper-making machine. 37 CFR 1.131 affidavit established use of electrostatic forces to adhere starch particles to wet blotting paper moved over a fluidized bed of starch particles prior to the applied reference date. Affidavit was sufficient in view of prior art reference showing that deposition of dry coatings directly on wet webs on the Fourdrinier wire of a paper-making machine was well known in the art prior to the date of the applied reference. The affidavit established possession of the basic invention, i.e., use of electrostatic forces to adhere starch to wet paper.).

SWEARING BEHIND ONE OF A PLURALITY OF COMBINED REFERENCES

Applicant may overcome a 35 U.S.C. 103 rejection based on a combination of references by showing completion of the invention by applicant prior to the effective date of any of the references; applicant need not antedate the reference with the earliest filing date. However, as discussed above, applicant's 37 CFR 1.131 affidavit must show possession of either the whole invention as claimed or something falling within the claim(s) prior to the effective date of the reference being antedated; it is not enough merely to show possession of what the reference happens to show if the reference does not teach the basic inventive concept.

Where a claim has been rejected under 35 U.S.C. 103 based on Reference A in view of Reference B, with the effective date of secondary Reference B being earlier than that of Reference A, the applicant can rely on the teachings of Reference B to show that the differences between what is shown in his or her 37 CFR 1.131 affidavit or declaration and the claimed invention would have been obvious to one of ordinary skill in the art prior to the date of Reference A. However, the 37 CFR 1.131 affidavit or declaration must still establish possession of the claimed invention, not just what Reference A shows, if Reference A does not teach the basic inventive concept.

GENERAL RULE AS TO GENERIC CLAIMS

A reference or activity applied against generic claims may (in most cases) be antedated as to such claims by an affidavit or declaration under 37 CFR 1.131 showing completion of the invention of only a single species, within the genus, prior to the effective date of the reference or activity (assuming, of course, that the reference or activity is not a statutory bar or a patent, or an application publication, claiming the same invention). See *Ex parte Biesecker*, 144 USPQ 129 (Bd. App. 1964). See, also, *In re Fong*, 288 F.2d 932, 129 USPQ 264 (CCPA 1961); *In re Defano*, 392 F.2d 280, 157 USPQ 192 (CCPA 1968) (distinguishing chemical species of genus compounds from embodiments of a single invention). See, however, MPEP § 715.03 for practice relative to cases in unpredictable arts.

715.03 Genus-Species, Practice Relative to Cases Where Predictability Is in Question

→ Where generic claims have been rejected on a reference or activity which discloses a species not antedated by the affidavit or declaration, the rejection will not ordinarily be withdrawn, subject to the rules set forth below, unless the applicant is able to establish

that he or she was in possession of the generic invention prior to the effective date of the reference or activity. In other words, the affidavit or declaration under 37 CFR 1.131 must show as much as the minimum disclosure required by a patent specification to furnish support for a generic claim.

REFERENCE OR ACTIVITY DISCLOSES SPECIES

A. Species Claim

Where the claim under rejection recites a species and the reference or activity discloses the claimed species, the rejection can be overcome under 37 CFR 1.131 directly by showing prior completion of the claimed species or indirectly by a showing of prior completion of a different species coupled with a showing that the claimed species would have been an obvious modification of the species completed by applicant. See *In re Spiller*, 500 F.2d 1170, 182 USPQ 614 (CCPA 1974).

B. Genus Claim

The principle is well established that the disclosure of a species in a cited reference is sufficient to prevent a later applicant from obtaining a "generic claim." *In re Gosteli*, 872 F.2d 1008, 10 USPQ2d 1614 (Fed. Cir. 1989); *In re Slayter*, 276 F.2d 408, 125 USPQ 345 (CCPA 1960).

Where the only pertinent disclosure in the reference or activity is a single species of the claimed genus, the applicant can overcome the rejection directly under 37 CFR 1.131 by showing prior possession of the species disclosed in the reference or activity. On the other hand, a reference or activity which discloses several species of a claimed genus can be overcome directly under 37 CFR 1.131 only by a showing that the applicant completed, prior to the date of the reference or activity, all of the species shown in the reference. *In re Stempel*, 241 F.2d 755, 113 USPQ 77 (CCPA 1957).

Proof of prior completion of a species different from the species of the reference or activity will be sufficient to overcome a reference indirectly under 37 CFR 1.131 if the species shown in the reference or activity would have been obvious in view of the species shown to have been made by the applicant. *In re Clarke*, 356 F.2d 987, 148 USPQ 665 (CCPA 1966); *In re Plumb*, 470 F.2d 1403, 176 USPQ 323 (CCPA 1973); *In re Hostettler*, 356 F.2d 562, 148 USPQ 514 (CCPA 1966). Alternatively, if the applicant cannot show possession of the species of the reference or activity in this manner, the applicant may be able to antedate the reference or activity indirectly by, for example, showing prior completion of one or more species which put him or her in possession of the claimed genus prior to the reference's or activity's date. The test is whether the species completed by applicant prior to the reference date or the activity's date provided an adequate basis for inferring that the invention has generic applicability. *In re Plumb*, 470 F.2d 1403, 176 USPQ 323 (CCPA 1973); *In re Rainer*, 390 F.2d 771, 156 USPQ 334 (CCPA 1968); *In re Clarke*, 356 F.2d 987, 148 USPQ 665 (CCPA 1966); *In re Shokal*, 242 F.2d 771, 113 USPQ 283 (CCPA 1957).

It is not necessary for the affidavit evidence to show that the applicant viewed his or her invention as encompassing more than the species actually made. The test is whether the facts set out in the affidavit are such as would persuade one skilled in the art that the applicant possessed so much of the invention as is shown in the reference or activity. *In re Schaub*, 537 F.2d 509, 190 USPQ 324 (CCPA 1976).

C. Species Versus Embodiments

References or activities which disclose one or more embodiments of a single claimed invention, as opposed to species of a claimed genus, can be overcome by filing a 37 CFR 1.131 affidavit showing prior completion of a single embodiment of the invention, whether it is the same or a different embodiment from that disclosed in the reference or

activity. See *In re Fong*, 288 F.2d 932, 129 USPQ 264 (CCPA 1961) (Where applicant discloses and claims a washing solution comprising a detergent and polyvinylpyrrolidone (PVP), with no criticality alleged as to the particular detergent used, the PVP being used as a soil-suspending agent to prevent the redeposition of the soil removed, the invention was viewed as the use of PVP as a soil-suspending agent in washing with a detergent. The disclosure in the reference of the use of PVP with two detergents, both of which differed from that shown in applicant's 37 CFR 1.131 affidavit, was considered a disclosure of different embodiments of a single invention, rather than species of a claimed genus); *In re Defano*, 392 F.2d 280, 157 USPQ 192 (CCPA 1968).

REFERENCE OR ACTIVITY DISCLOSES CLAIMED GENUS

In general, where the reference or activity discloses the claimed genus, a showing of completion of a single species within the genus is sufficient to antedate the reference or activity under 37 CFR 1.131. *Ex parte Biesecker*, 144 USPQ 129 (Bd. App. 1964). In cases where predictability is in question, on the other hand, a showing of prior completion of one or a few species within the disclosed genus is generally not sufficient to overcome the reference or activity. *In re Shokal*, 242 F.2d 771, 113 USPQ 283 (CCPA 1957). The test is whether the species completed by applicant prior to the reference date or the date of the activity provided an adequate basis for inferring that the invention has generic applicability. *In re Mantell*, 454 F.2d 1398, 172 USPQ 530 (CCPA 1973); *In re Rainer*, 390 F.2d 771, 156 USPQ 334 (CCPA 1968); *In re DeFano*, 392 F.2d 280, 157 USPQ 192 (CCPA 1968); *In re Clarke*, 356 F.2d 987, 148 USPQ 665 (CCPA 1965). In the case of a small genus such as the halogens, which consists of four species, a reduction to practice of three, or perhaps even two, species might show possession of the generic invention, while in the case of a genus comprising hundreds of species, reduction to practice of a considerably larger number of species would be necessary. *In re Shokal, supra*.

It is not necessary for the affidavit evidence to show that the applicant viewed his or her invention as encompassing more than the species he or she actually made. The test is whether the facts set out in the affidavit are such as would persuade one skilled in the art that the applicant possessed so much of the invention as is shown in the reference. *In re Schaub*, 537 F. 509, 190 USPQ 324 (CCPA 1976).

715.04 Who May Make Affidavit or Declaration; Formal Requirements of Affidavits and Declarations

WHO MAY MAKE AFFIDAVIT OR DECLARATION

The following parties may make an affidavit or declaration under 37 CFR 1.131:

- (A) All the inventors of the subject matter claimed.
- (B) An affidavit or declaration by less than all named inventors of an application is accepted where it is shown that less than all named inventors of an application invented the subject matter of the claim or claims under rejection. For example, one of two joint inventors is accepted where it is shown that one of the joint inventors is the sole inventor of the claim or claims under rejection.
- (C) A party qualified under 37 CFR 1.42, 1.43, or 1.47 in situation where some or all of the inventors are not available or not capable of joining in the filing of the application.
- (D) The assignee or other party in interest when it is not possible to produce the affidavit or declaration of the inventor. *Ex parte Foster*, 1903 C.D. 213, 105 O.G. 261 (Comm'r Pat. 1903).

Affidavits or declarations to overcome a rejection of a claim or claims must be made